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Attorney Docket No. ARB001 CON/CIP
Client/Matter No. 86388.0004.002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Confirmation No.:
Jon M. Huppenthal and D. James Guzy	Group Art Unit:
Serial No. ----------	Examiner:
Filed: Herewith	
For: RECONFIGURABLE PROCESSOR MODULE COMPRISING HYBRID STACKED INTEGRATED CIRCUIT DIE ELEMENTS	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.97, the Examiner may wish to consider the references listed on the attached Form PTO/SB/08A. In submitting these references, no representation is made or implied that the references are or are not material to the examination of this application. Pursuant to 37 C.F.R. 1.98(d), copies of the references are not enclosed, as each reference was either provided or cited in U.S. Serial No. 10/452,113, from which priority under 35 U.S.C. 120 is claimed.

This Information Disclosure Statement is filed before mailing of a first Office Action in the above case. Accordingly, no fee is believed due. However, any fee associated herewith may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

3/15/04
Date

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Substitute for form 1449A/PTO				Application Number	----------
				Filing Date	**Herewith**
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				First Named Inventor	**Jon M. Huppenthal et al.**
				Art Unit	
(Use as many sheets as necessay)				Examiner Name	
Sheet	1	of	2	Attorney Docket No.	**ARB001 CON/CIP**

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Document No. No. – Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-6,449,170	**09/2002**	**Nguyen et al.**	
		US-6,051,887	**04/2000**	**Hubbard, Robert L.**	
		US-6,313,522	**11/2001**	**Akram et al.**	
		US-5,838,060	**11/1998**	**Comer, Alan E.**	
		US-6,092,174	**07/18/2000**	**Roussakov**	**Entire document**
		US-5,585,675	**12/17/1996**	**Knopf**	**Entire document**
		US-5,652,904	**06/29/1997**	**Trimberger**	**Entire document**
		US-6,072,233	**06/06/2000**	**Corisis et al.**	
		US-6,451,626	**09/17/2002**	**Lin**	
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FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns. Lines Where Relevant Passages or Relevant Figures Appear	T[6]

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published	T[2]
		HINTZKE, JEFF, Probing Thin Wafers Requires Dedicated Measures, http://www.eletroglas.com/products/White%20Paper/Hintzke_Thin_Paper.html, Electroglas, Inc. Aug. 21, 2001, pp. 1-6.	
		LAMMERS, DAVID, AMD, LSI Logic will put processor, flash in single package, http://www..csdmag.com/story/OEG20001023S0039, EE Times, Aug. 21, 2001, pp.1-2.	
		Multi-Adaptive Processing (MAP™), http://www.srccomp.com/products_map.htm, SRC Computers, Inc. Aug. 22, 2001, pp.1-2.	
		System Architecture, http://www.srccomp.com/products.htm, SRC Computers, Inc., Aug. 22, 2001, pp.1-2.	
		Configurations, SRC Expandable Node, http://www.srccomp.com/products_configs.htm, SRC Computers, Inc. Aug. 22, 2001, p.1.	
		YOUNG, JEDEDIAH J., MALSHE, AJAY P., BROWN, W.D., LENIHAN, TIMOTHY, ALBERT, DOUGLAS, OZGUZ, VOLKAN, Thermal Modeling and Mechanical Analysis of Very Thin Silicon Chips for Conformal Electronic Systems, University of Arkansas, Fayetteville, AR, pp.1-8.	
		New Process Forms Die Interconnects by Vertical Wafer Stacking, http://www.chipscalereview.com/0001/technews8.html, ChipScale Review, January-February 2000, Oct. 18, 2001, pp. 1-3.	
		SAVASTIOUK, SERGEY, SINIAGUINE, OLEG, FRANCIS, DAVID, Thinning Wafers for Flip Chip Applications, http://www.iii1.com/hdiarticle.html, International Interconnection Intelligence, Oct. 18, 2001, pp. 1-13.	
		SAVASTIOUK, SERGEY, SINIAGUINE, OLEG, KORCZYNSKI, ED, Ultra-thin Bumped and Stacked WLP using Thru-Silicon Vias, http://www.ectc.net/advance_program/abstracts2000/s15p1.html, Tru-Si Technologies, Inc., Oct. 18, 2001, p. 1.	
		SAVASTIOUK, SERGEY, New Process Forms Die Interconnects by Vertical Wafer Stacking, http://www.trusi.com/article9.htm, ChipScale Review, Oct. 18, 2001, pp.1-2.	
		SAVASTIOUK, SERGEY, Moore's Law- the z dimension, http://www.trusi.com/article7.htm, SolidState Technology, Oct. 18, 2001, pp. 1-2.	
		Through-Silicon Vias, http://www.trusi.com/throughsiliconvias.html, Tru-Si Technologies, Oct. 18, 2001, p. 1.	

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